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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,212	03/29/2002	Robert L. Barry	BUR920010182	7089

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FREDERICK W. GIBB, III
MCGINN & GIBB, PLLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

DK

Office Action Summary	Application No.	Applicant(s)	
	10/063,212	BARRY ET AL.	
	Examiner	Art Unit	
	Ly D Pham	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 May 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

FINAL REJECTION

DETAILED ACTION

1. Applicants' Amendment A has been entered in Office Paper No. 7, in which claims 21 – 26 are canceled and claims 1 – 3, 8 – 10, and 15 – 17 have been amended.

Drawings

2. This application, filed under former 37 CFR 1.60, lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US Pat Pub 2002/0171101 A1) in view of Holst (US Pat 6,054,918).

Regarding **claims 1, 8, and 15**, Hsu et al. disclose a memory cell connected to true bitline and a complement bitline, said memory cell comprising:

a first transistor having a first drain (fig. 2, transistor 14); and a second transistor having a second drain (fig. 2, transistor 18), wherein said first drain is connected to said true bitline (transistor 14 with first drain connected to BL0—true bit line) and said second drain is connected to said complement bitline (transistor 18 with second drain connected to BL0'—complement bitline), wherein said first transistor further comprises a first source, and said second transistor further comprises a second source (fig. 2, both transistors 14 and 18 have its own source).

Although Hsu et al. did not further show the feature wherein only one of the first source and the second source is connected to ground, it is however shown by Holst in figure 8 (take for example a pair of complementary memory cells 804 and 806, only the source of transistor 804 is connected to ground). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to include the feature shown by Holst to the disclosure of Hsu et al. to improve speed (col. 13, lines 23 – 29).

The memory structure shown by Hsu et al. is a flash type memory, nevertheless, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to realize its possible design for ROM type, as claimed, as read-only becomes another desirable and applicable arrangement (col. 5, paragraph 0062).

Regarding claims **2, 9, and 16**, Holst also discloses the memory cell in claims 1, 8, and 15, wherein a connection of one of said first source and said second source to a ground programs said ROM cell (fig. 8, the configuration of memory cell 808 programs it).

Regarding **claims 4 and 11**, the examiner takes an Official Notice that the claimed feature in these claims, namely, the connection of the memory cell in claim 2 comprises an electrical connection formed during manufacturing of said first and second transistors, is considered common and well known in the memory art, as memory chips are manufactured with processes including forming electrical connections (as part of metal layers) being well known in the art.

Regarding **claims 5, 12, and 18**, Hsu et al. further show the memory cell in claim 1, wherein both the gates of the first and second transistors are connected to a wordline (fig. 2, gates of transistors 14 and 18 are both connected to wordline WL0).

Regarding **claims 6, 13, and 19**, Hsu et al. also show the memory cell in claim 1, wherein said second transistor comprises a complement transistor to said first transistor (second transistor 18 is complement to first transistor 14).

Regarding **claims 4, 7, and 20**, Hsu et al. also show the memory cell in claim 1, wherein said memory cell shares said first drain and said second drain with corresponding drains of an adjacent memory cell in said array (in the memory array of fig. 2, drain of first transistor 14 shares the bitline BL0 with the adjacent transistor right below it and drain of second transistor 18 shares the bitline BL0' with the adjacent transistor right below it).

5. The indicated allowability of claims 3, 10, and 17 is withdrawn in view of the newly discovered reference(s) to Holst (US Pat 6,054,918). Rejections based on the newly cited reference(s) follow.

Regarding **claims 3, 10, and 17**, Holst further shows in fig. 8 that only one of the first source and second source is connected to the ground (transistor 804) and the other of the first source and second source is insulated from electrical connections (transistor 806).

Conclusion

6. When responding to the office action, Applicant(s) are advised to provide the examiner with the page and line numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

8. Any inquiry concerning this communication on earlier communications from the examiner should be directed to Ly Pham, whose telephone number is 703-305-4862. The examiner can normally be reached on Monday – Friday from 8:30am to 5:00pm, alternate Friday off. The examiner's supervisor, David Nelms, can be reached at 703-308-4910. The fax number for the organization where this application or proceeding is assigned is 703-308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Ly Pham

August 1, 2003

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PRIMARY EXAMINER